REMARKS

Claims 1 through 27 are pending.

Claims 1, 12 and 20 have been amended to more distinctly claim the invention. Support for the amendment can be found, for example, at page 8, lines 1 through 7.

Attached hereto is a marked up version of the changes made to the claims by the current amendment. The attached pages are captioned "Version with Markings to Show Changes Made."

No new matter has been added.

The Applicants respectfully request reconsideration of the present application in view of the above amendments and the following remarks. Some of the technical differences between the applied references and embodiments of the invention will now be discussed. Of course, these discussed differences regarding the embodiments, which are disclosed in detail in the specification do not define the scope or interpretation of any of the claims. Instead, when presented, such differences are offered merely to help the Examiner appreciate important claim distinctions as they are discussed.

Objection to Title of the Invention

The title of the invention is objected to as not being descriptive. The Examiner suggests that the title be changed to "Apparatus for measuring features of a semiconductor device". The title of the invention has been amended, thereby obviating the basis for this objection.

Reconsideration and withdrawal of this objection is respectfully requested.

Objection to Claims 5-8 and 24-27

Claims 5-8 and 24-27 are objected to as being misleading. The Examiner states that the phrase "one of the support" implies more than one claimed support. Applicants respectfully traverse the objection.

The phrase "one of the support" must be viewed in context of the remaining portion of the claim; that is, "one of the support and the source to detect movement of the one of the support and the source". In this context, the phrase refers to either the support or the source, not to multiple supports. One skilled in the art, when reading the entire claim, would understand to what the phrase refers to.

Reconsideration and withdrawal of this objection is respectfully requested.

Rejection of Claims 1-11 under 35 U.S.C. § 112, First Paragraph

Claims 1-11 are rejected under 35 U.S.C. § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains to make and/or use the invention. The Examiner continues that the phrase "first and second depths" describes a mechanism of providing simultaneous irradiation with a beam of different foci, wherein applicant's [sic] disclosure does not disclose such a mechanism. Applicants respectfully traverse this rejection.

Generally, the disclosed invention is directed towards an apparatus useful for determining the three-dimensional profile(s) of a semiconductor device, i.e., a silicon chip. For example, in one aspect of the invention, the controller 70 controls the electron gun 30 and the lenses 31 and 33 to produce an electron beam 34 having a selected depth of focus. The drive unit 42 moves the stage 40 into position beneath the electron gun 30 and ***moves the stage in the Z direction so that the electron beam 34 is focused on a selected portion of the semiconductor substrate 20.*** The drive unit 42 then moves the stage 40 in the X and Y directions to scan the electron beam 34 in a series of parallel paths across the semiconductor substrate 20, producing the secondary beams 51 that are received by the electron detectors 50 and processed by the processor 73.

Figure 2A is a side elevation view of an example of the semiconductor substrate 20. In the embodiment shown in Figure 2A, the semiconductor substrate 20 has a top surface 22, a bottom

surface 27, and two raised features 21 projecting above the top surface 22. In other embodiments, the semiconductor substrate 20 may have more than two features and/or may have features that are recessed from the top surface 22. Each feature 21 has an upper surface 23, upper corners 25 (shown as 25a and 25b), side surfaces 24 (shown as 24a and 24b), and lower corners 26 (shown as 26a and 26b).

The semiconductor substrate may be scanned by ***a first electron beam 34'*** having a ***depth of focus D1*** centered on the upper corners 25 of the features 21, and by ***a second electron beam 34''*** having a ***depth of focus D2*** centered on the lower corners 26 of the feature. When the first electron beam 34' scans across the semiconductor substrate 20, the detectors 50 (Figure 1) generate a series of electrical signals corresponding to the secondary beams 51 (Figure 1). Figure 2B is a plan view of a two-dimensional image 52 generated from the signals and having a pattern of contrasting regions corresponding to the features 21 and the top surface 22 of the semiconductor substrate 20. As shown in Figure 2B, dark regions 54 correspond to the substrate top surface 22, light regions 53 correspond to the side surfaces 24 of the features 21, and gray regions 55 correspond to the upper surfaces 23 of the features. (Emphasis added.)

Thus, by positioning the semiconductor device at different distances from the electron beam, different profiles of the semiconductor device can be obtained. The information generated by the reflected electrons can be used to graphically represent the three-dimensional features of the semiconductor device. By use of two or more depths of electron beam penetration, the profile of the semiconductor device can be developed along multiple depths of penetration as desired. Therefore, one skilled in the art would be enabled to make and use the invention in view of the teachings of the specification.

Reconsideration and withdrawal of this rejection is respectfully requested.

Rejection of Claims 1-4 and 11 under 35 U.S.C. § 102(b)

Claims 1-4 and 11 are rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 4,600,839, issued to Ichihasi et al. (hereinafter "Ichihashi et al."). Applicants respectfully traverse this rejection.

In one embodiment, the disclosed invention is an apparatus for determining a dimension of a feature of a semiconductor device. The apparatus includes at least one source of electrons, a focusing device and a support. The focusing device is positioned proximate to the source of electrons to focus electrons emitted by the source and form an electron beam. The focusing device focuses the electron beam to a first depth and then a second depth of focus to form at least one representation of the semiconductor device corresponding to electrons focused at the first and second depths of focus and impinging on the semiconductor device. The support is aligned with the electron beam and includes a support surface to engage the semiconductor device and support the semiconductor device. Either one of the electron beam and the support are movable relative to the other ***in any of the x, y, or z planes***.

In contrast to the present invention, Ichihashi et al. disclose an apparatus to measure the profile of a semiconductor device in ***only the x and y planes***. For example, Ichihashi et al. describe the apparatus and method of profiling a semiconductor chip in terms of one or two dimensions, i.e., X and Y planes (column 2, line 68 through column 3, line 4). More specifically, Ichihashi et al. disclose that "it is desired to measure the dimensions in two orthogonal (X, Y) directions" (column 3, lines 61 through 62). Ichihashi et al. do not teach or suggest and fail to appreciate that multiple irradiations of a semiconductor device surface at various depths of penetration (in the Z direction) would produce any

useful information.

Therefore, claim 1 is in an allowable form. Claims 2-4 and 11 that depend from claim 1 are similarly allowable based upon the allowability of claim 1 and further in view of the additional limitations recited in the dependent claims.

Reconsideration and withdrawal of this rejection is respectfully requested.

Rejection of Claims 5-8 under 35 U.S.C. § 103(a)

Claims 5-8 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Ichihashi et al. as applied to claim 1-4 above, and further in view of U.S. Patent No. 4,447,731, issued to Kuni et al. (hereinafter "Kuni et al."). Applicants respectfully traverse this rejection.

The discussions and arguments set forth above with regard to the teachings of Ichihashi et al. are incorporated in their entirety and are reiterated here.

Claim 5, indirectly dependent from independent claim 1, pertains to use of a third detector operatively coupled to either the support or the source to detect movement of the support or the source to generate a third signal which corresponds to the movement detected.

Claim 6, dependent from dependent claim 5, further provides a memory device coupled to at least one of the detectors to store the signal generated by the detector. Claim 7, dependent from dependent claim 5, provides for graphically displaying the voltage generated by the first and second electron flows of electrons. Claim 8, also dependent from dependent claim 5, is directed to a printing

device that prints a representation of the voltage generated by the first and second electron flows of electrons as a function of the movement detected by the third sensor.

Kuni et al. do not remedy the deficiencies of Ichihashi et al. Kuni et al disclose an apparatus for determining the profile of a semiconductor wafer by passing a single electron beam across the surface of the object. Kuni et al. fail to teach or suggest that multiple electron beams focused at different depths of focus, and hence, two or more depths of focus of electron beams could provide useful information regarding the three-dimensional aspects of the semiconductor wafer. As the Examiner states, Kuni et al do not teach a memory device, a voltage display or a print device. These are important aspects of the invention that are linked to the ability of the apparatus to profile depths of semiconductor devices by use of multiple electron beams focused at varying depths that impinge on the semiconductor device surface.

Neither Ichihashi et al. or Kuni et al., alone or in combination, teach or suggest, provide any motivation or an expectation of success to one having ordinary skill in the art that an apparatus that utilizes multiple focused electron beams could be used to determine the three-dimensional profile of a semiconductor device. Therefore, neither Ichihashi et al. nor Kuni et al., alone or in combination, teach or suggest to one having ordinary skill in the art that the measurement of two or more depths of focus of multiple electron beams could be used with a memory device to store the signals, or to display the voltages or to print a representation of the voltage generated by the first and second flows of electrons as a function of the movement detected by a third sensor.

Therefore, claims 5-8 are in allowable form. Reconsideration and withdrawal of the pending rejection is respectfully requested.

Rejection of Claims 9, 10 and 12-27 under 35 U.S.C. § 103(a)

Claims 9, 10 and 12-27 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Ichihashi et al. as applied to claim 1 above, and further in view of U.S. Patent No. 5,006,795, issued to Yoshizawa et al. (hereinafter "Yoshizawa et al."). Applicants respectfully traverse this rejection.

The discussions and arguments set forth above with regard to the teachings of Ichihashi et al. are incorporated in their entirety and are reiterated here.

Yoshizawa et al. do not remedy the deficiencies of Ichihashi et al. Yoshizawa et al. describe an apparatus that focuses two electron beams of energy onto a target at one position. Both electron beams taught by Yoshizawa et al. are directed to the same depth of penetration at a given position along an x/y axis. Yoshizawa et al. do not teach or suggest that the two electron beams could be focused at a first depth and a second depth. Moreover, Yoshizawa et al. do not teach or suggest that the semiconductor device could be positioned along the Z axis but only along the x and y axis.

Neither Ichihashi et al. or Yoshizawa et al., alone or in combination, teach or suggest, provide any motivation or an expectation of success such that one having ordinary skill in the art would utilize an apparatus that focuses an electron beam to a first depth and then a second depth as embodied by the current invention. Neither Ichihashi et al. or Yoshizawa et al., alone or in combination, teach or suggest, provide any motivation or an expectation of success to one having ordinary skill in the art that two electron beams could be focused at two different depths of penetration to visualize the profile of a semiconductor device in three-dimensions.

The conclusion that "one skilled in the art with this available common knowledge could clearly

reason the claimed invention..." evidences the Examiner's application of an improper legal standard, i.e., hindsight. Moreover, as the Examiner states in the rejection under 35 U.S.C. § 112, first paragraph, that "it is not obvious to one skilled in the art how to achieve such an effect." The Examiner is not permitted to pick and choose from any one reference only so much as of it as will support a given position.

The Court of Appeals for the Federal Circuit has strongly criticized the practice of basing obviousness analyses on hindsight, remarking:

> Our case law makes clear that the best defense against the subtle but powerful attraction of a hindsight-based obviousness analysis is rigorous application of the requirement for a showing of the teaching or motivation to combine prior art references. See, e.g., C.R. Bard, Inc. v. M3 Sys., Inc., 157 F.3d 1340, 1352, 48 USPQ2d 1225, 1232 (Fed. Cir. 1998) (describing "teaching or suggestion or motivation [to combine]" as an "essential evidentiary component of an obviousness holding"); In re Rouffet, 149 F.3d 1350, 1359, 47 USPQ2d 1453, 1459 (Fed. Cir. 1998) ("the Board must identify specifically . . . the reasons one of ordinary skill in the art would have been motivated to select the references and combine them"); In re Fritch, 972 F.2d 1260, 1265, 23 USPQ2d 1780, 1783 (Fed. Cir. 1992) (examiner can satisfy burden of obviousness in light of combination "only by showing some objective teaching [leading to the combination]"); In re Fine, 837 F.2d 1071, 1075, 5 USPQ2d 1596, 1600 (Fed. Cir. 1988) (evidence of teaching or suggestion "essential" to avoid hindsight); Ashland Oil, Inc. v. Delta Resins & Refractories, Inc., 776 F.2d 281, 297, 227 USPQ 657, 667 (Fed. Cir. 1985) (district court's conclusion of obviousness was error when it "did not elucidate any factual teachings, suggestions or incentives from this prior art that showed the propriety of combination"). See also Graham, 383 U.S. at 18, 148 USPQ at 467 ("strict observance" of factual predicates to obviousness conclusion

> required). Combining prior art references without evidence of such a suggestion, teaching, or motivation simply takes the inventor's disclosure as a blueprint for piecing together the prior art to defeat patentability–the essence of hindsight. See, e.g., Interconnect Planning Corp. v. Feil, 774 F.2d 1132, 1138, 227 USPQ 543, 547 (Fed. Cir. 1985) ("The invention must be viewed not with the blueprint drawn by the inventor, but in the state of the art that existed at the time.").

In re Dembiczak, 50 USPQ2d 1614, 1617 (Fed. Cir. 1999). Here the Examiner has failed to adhere to the standards mandated by the Federal Circuit in conducting an analysis attempting to show that the claims are obvious because "[b]road conclusory statements regarding the teaching of multiple references, standing alone, are not 'evidence'" *Id.*

For at least these reasons, Applicants respectfully assert that the art cited by the Examiner, alone or in combination, does not teach or suggest, or provide any motivation or an expectation of success to arrive at the present invention as embodied by the pending claims. Reconsideration and withdrawal of the rejection under 35 U.S.C. § 103(a) is respectfully requested.

Conclusion

In view of the foregoing, Applicants submit that all pending claims distinguish over all references cited by the Examiner and respectfully requests that all rejections be withdrawn. The Examiner is invited to telephone the undersigned attorney for Applicants in the event that such communication is deemed to expedite prosecution of this application.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

1. (Amended) An apparatus for determining a dimension of a feature of a semiconductor device, comprising:

at least one source of electrons;

a focusing device positioned proximate to the source of electrons to focus electrons emitted by the source and form an electron beam, the focusing device focusing the electron beam to have a first depth and a second [depths] depth of focus and form at least one representation of the semiconductor device corresponding to electrons focused at the first and second depths of focus and impinging on the semiconductor device;

a support aligned with the electron beam and having a support surface to engage the semiconductor device and support the semiconductor device, one of the electron beam and the support being movable relative to the other of the electron beam and the support in any of the x, y, or z planes.

12. (Amended) An apparatus for determining a dimension of a feature of a semiconductor device, comprising:

a source of electrons;

a port surface having a first and second ports therethrough, the first port being positioned proximate to the source to form a first electron beam when electrons pass therethrough, the second port spaced apart from the first port to form a second electron beam when electrons pass therethrough;

a first focusing device positioned proximate to the first port and adjacent the first electron beam to focus the first electron beam on a first position;

a second focusing device positioned proximate to the second port and adjacent the second electron beam to focus the second electron beam on a second position that is different from the first position; and

a support aligned with the first and second ports and having a support surface to engage the semiconductor device and support the semiconductor device at the first and second positions, one of the support and the source being movable relative to the other of the support and the source in any of the x, y, or z planes.

20. (Amended) An apparatus for determining a dimension of a semiconductor device feature, comprising:

first and second sources of electrons;

a first focusing device positioned proximate to the first source of electrons to focus a first electron beam emitted from the first source;

a second focusing device positioned proximate to the second source of electrons to focus a second electron beam emitted from the second source; and

a support aligned with the first and second focusing devices and configured to engage the semiconductor device, one of the support and the sources of electrons being movable relative to the other of the support and the sources of electrons in any of the x, y, or z planes.